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## Ice Lake 3rd Generation Xeon Scalable

## Processors



What is Ice Lake Xeon Scalable?

The Ice Lake Xeon (ICX) Scalable Processor (ICL-SP) line is Intel's 3rd Generation of Xeon processors, generationally succeeding the previous 2nd generation, 14 nm Cascade Lake (CSL/CLX) microarchitecture. Cascade Lake, for its part, was based off of the Skylake microarchitecture as an Optimization phase in Intel's Process-Architecture-Optimization (PAO) development model. Ice Lake forms one-half of the 3rd Generation, utilizing Sunny Cove cores, with the other half being the 14 nm Cooper Lake (CPL) microarchitecture, also designed to succeed Cascade Lake but in a different fabrication process node. The $10 \mathrm{~nm}+$ node does have some advantages over 14 nm such as higher density scaling, thanks to various production improvements. Ice Lake is therefore the leading edge of this particular generation, designed to add new features and maximum performance for the Xeon lineup as a complete platform solution.

ICL-SP has four tiers of processors: Silver, Gold 5300, Gold 6300, and Platinum. Silver comes with 8 to 20 cores and a thermal design power (TDP) range of 105-150W, 8GB of Intel's Software Guard Extensions (SGX) per central processing unit (CPU), but lacking Intel DC Persistent Memory Module (DCPMM) support except for the 4314 model. The Gold 5300 tier has 8 to 26 cores with a TDP of $140-185 \mathrm{~W}, 64 \mathrm{~GB}$ of SGX per CPU with 512GB on the 5318 , and DCPMM support. The Gold 6300 tier has 8 to 32 cores with $165-235$ TDP and 64GB SGX per CPU, also with DCPMM support. Lastly, the Platinum tier has 32 to 40 cores at 185270 W with 8,64 , or 512GB SGX depending on the model, with DCPMM support. Models with 8 to 28 cores are known as high core count (HCC) while those from 16 to 40 are extreme core count (XCC). Models are divided into their area of specialization, whether it be for 4 - and 8 -socket solution scaling or the highest percore performance.

ICL-SP processors have a peak single-thread turbo of 3.7 GHz and multi-thread turbo of 3.6 GHz , lower than the previous generation but more than compensated for with instruction per clock (IPC) gains and a higher core count. Intel has several specializations in the ICL lineup including for liquid-cooled, uniprocessor-only, Intel Speed Select Technology Power Profile (SST-PP) 2.0 support, 512GB SGX per CPU guaranteed, and long-life with extended thermal support. SST-PP includes improvements to base and turbo frequencies with Core Power assistance to improve peak per-core performance with better quality of service (QoS), utilizing independent power management agents. Additionally, there are models optimized for infrastructure as a service (laaS), software as a service (SaaS), networking and network functions virtualization, as well as media processing.

These processors require a new motherboard utilizing the LGA4189-4 "Whitley" socket, as distinct from Cooper Lake's LGA4189-5 "Cedar Island" socket. These two microarchitectures have a lot in common and the optimizations listed above are very much centered around getting the most out of storage, particularly solid state. $\mathrm{NVMe}^{\mathrm{Tm}}$ drives, especially moving forward, will leverage network virtualization within, for example, a hybrid cloud solution using laaS and SaaS. This is especially true with the potential of tiered DCPMM, with the extra cores and IPC offering better efficiency for storage utilization across the stack. Check out our hybrid cloud blog for more information on the former.

## Generational Hardware and Platform Improvements

ICL-SP has a maximum core count of 40 versus CSL's 28, or 80 threads from 56, along with $48 \mathrm{~KB} / 1.25 \mathrm{MB} / 1.5 \mathrm{MB}$ of $\mathrm{L} 1 / \mathrm{L} 2 / \mathrm{L} 3$ cache per core, up from $32 \mathrm{~KB} / 1 \mathrm{MB} / 1.375 \mathrm{MB}$ per core with a larger Translation Lookaside Buffer (TLB). ICL-SP also has 8-channel memory support up from 6-channel, in single DIMM per channel ( 1 DPC) at 3200 or dual ( 2 DPC ) at $2933 \mathrm{MT} / \mathrm{s}$. Also supported is up to 4 TB of memory per socket, versus 1TB with CSL. The Intel Ultra Path Interconnect (UPI) transfer rate has increased from 10.4 GT/s to $11.2 \mathrm{GT} / \mathrm{s}$ for faster inter-core communication, with $3 x$ UPI support. The CPUs can now address 64 lanes of peripheral component interconnect express ( $\mathrm{PCle®}$ ), up from 48 , as well as doubling the bandwidth per lane by going from PCle 3.0 to $\mathrm{PCle®}$ 8.0.

The re-order buffer has increased from 224 to 352 entries which allows for improved out-of-order execution. The amount of micro-operations ( $\mu \mathrm{\rho ps}$ ) that can be tracked include 128 in-flight with 72 stored, up from 72 and 56, respectively. Scheduler entries have increased from 97 to 160, and register files integer and floating point, respectively - have increased from 180 and 168 to 280 and 224, also respectively. The allocation queue has also improved from 64 per thread to 70 per thread. These and other improvements, such as the larger caches mentioned above, in tandem with the smaller process node, help lead to significant IPC improvements.

Of particular value to storage is the vast increase in PCle ® bandwidth, both from a greater number of lanes and the move to PCle® 4.0. This, along with the Intel C620A chipset, provides a ton of storage options with
a much higher threshold for bottlenecking. Storage also benefits from improved Optane DC Persistent Memory (ODCPM) support, specifically the 200-series known as Barlow Pass. This allows for a flexible hierarchy between main memory and traditional non-volatile storage, regardless of form factor. Our content distribution network and SATA blog entries may provide further information.

## Application-Specific and Platform Improvements

ICL-SP promises a $20 \%$ IPC performance uplift, mirroring the $18 \%$ seen with Ice Lake in mobile, with larger gains in memory-limited situations not least thanks to higher memory bandwidth as well as new memory prefetch and optimization. This includes an updated instruction set architecture (ISA) including the addition of vector AES (vAES), Galois Field New Instructions (GFNI), secure hash algorithm (SHA) via SHA-NI extensions, the vector bit manipulation instruction (VBMI), cryptographic algorithm support, improved AVX512 with VPMADD52 for big-number arithmetic, Vector Carryless Multiply, and more. These additions provide large improvements to ICL-SP over CSL especially with regard to Intel's Crypto Acceleration. Intercore improvements also exist with upgraded algorithms with smarter balancing between instructions and power draw, leading to higher gains with larger-bit instructions.

Beyond crypto acceleration, there are vast improvements in AI with up to 74\% faster AI performance including AI inference. This includes the addition of Intel's Deep Learning Boost (DLBoost). Intel is also going for a unified ecosystem through the oneAPI programming model with Agilex FPGA support, SmartNIC support including 800-series Ethernet, Intel Internet of Things (IoT) Market Ready Solutions and Intel Select Solutions. There is also a push of improvements for high performance computing (HPC). These are all growing areas with the need for faster, more reliable storage, as detailed in our IoT, HPC, and edge computing blog entries, as well as our SR-IOV white paper. Intel has options focused on both node scaling and per-core performance, which ties directly into the future of flexible $\mathrm{NVMe}^{T w}$ storage as defined in this literature.

Intel also has security improvements, the most pertinent being Software Guard Extensions, or SGX, enclaves. These are private regions of memory that are protected with security instruction codes to prevent outside access regardless of privilege level. This essentially utilizes the CPU to encrypt portions of memory
to protect against potentially hostile access. Not all ICL processor models support this, and the amount of memory that can be managed by each core varies with specific model, as mentioned above. Intel also includes Total Memory Encryption (TME) and Intel's Platform Firmware Resilience (PFR) to further improve security.

## Summary

Intel's new Ice Lake Xeon Scalable Processors offer a wide range of solutions coupled with new features and a more capable platform. Improvements to IPC, memory bandwidth, and core count are bolstered by the addition of multimedia and AI algorithms as well as persistent memory support. Intel's unified approach means an entire ecosystem can be built around ICL, and all of it is defined by storage. All-flash arrays (AFA) provide the storage for big data and, along with Intel's fast Xeon processors, can bring latency down to a minimum without compromising on efficiency. Whether you're building for laaS, SaaS, a hybrid cloud, or going for cutting-edge network virtualization, Intel has you covered with both scalable and per-core performance processor solutions. And Solid State Storage Technology Corp. has you covered for the storage that drives these implementations, whether big or small.
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